12-Bit, 105 MSPS/125 MSPS IF Sampling A/D Converter

AD9433

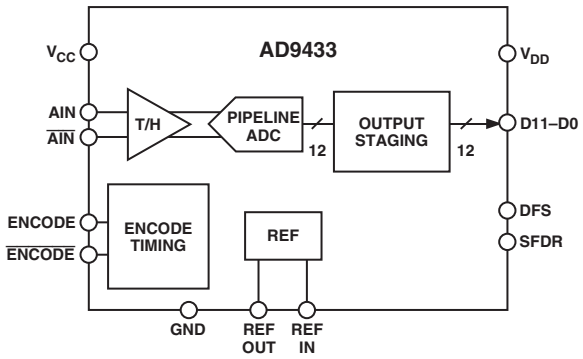
FEATURES

IF Sampling up to 350 MHz
SNR = 67.5 dB, f_{IN} up to Nyquist @ 105 MSPS
SFDR = 83 dBc, f_{IN} 70 MHz @ 105 MSPS
SFDR = 72 dBc, f_{IN} 150 MHz @ 105 MSPS
2 V p-p Analog Input Range Option
On-Chip Clock Duty Cycle Stabilization
On-Chip Reference and Track/Hold
SFDR Optimization Circuit
Excellent Linearity:
DNL = ±0.25 LSB (Typ)
INL = ±0.5 LSB (Typ)
750 MHz Full Power Analog Bandwidth
Power Dissipation = 1.35 W Typical @ 125 MSPS
Two's Complement or Offset Binary Data Format
5.0 V Analog Supply Operation
2.5 V to 3.3 V TTL/CMOS Outputs

APPLICATIONS

Cellular Infrastructure Communication Systems
3G Single and Multicarrier Receivers
IF Sampling Schemes
Wideband Carrier Frequency Systems
Point to Point Radios
LMDS, Wireless Broadband
MMDS Base Station Units
Cable Reverse Path
Communications Test Equipment
Radar and Satellite Ground Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL INTRODUCTION

The AD9433 is a 12-bit monolithic sampling analog-to-digital converter with an on-chip track-and-hold circuit and is designed for ease of use. The product operates up to 125 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband and high IF carrier systems.

The ADC requires a 5 V analog power supply and a differential encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic.

A user-selectable, on-chip proprietary circuit optimizes spurious-free dynamic range (SFDR) versus signal-to-noise-and-distortion (SINAD) ratio performance for different input signal frequencies, providing as much as 83 dBc SFDR performance over the dc to 70 MHz band.

The encode clock supports either differential or single-ended input and is PECL-compatible. The output format is user-selectable for binary or two's complement and provides an overrange (OR) signal.

Fabricated on an advanced BiCMOS process, the AD9433 is available in a thermally enhanced 52-lead plastic quad flatpack specified over the industrial temperature range (–40°C to +85°C) and is pin-compatible with the AD9432.

PRODUCT HIGHLIGHTS

1. IF Sampling
   The AD9433 maintains outstanding ac performance up to input frequencies of 350 MHz. Suitable for 3G Wideband Cellular IF sampling receivers.
2. Pin-Compatibility
   This ADC has the same footprint and pin layout as the AD9432, 12-Bit 80/105 MSPS ADC.
3. SFDR Performance
   A user-selectable on-chip circuit optimizes SFDR performance as much at 85 dBc from dc to 70 MHz.
4. Sampling Rate
   At 125 MSPS, this ADC is ideally suited for current wireless and wired broadband applications such as LMDS/MMDS and cable reverse path.

REV. 0

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AD9433–SPECIFICATIONS

DC SPECIFICATIONS (V_{DD} = 3.3 V, V_{CC} = 5 V; internal reference; differential encode input, unless otherwise noted.)

Parameter	Temp	Test Level	AD9433BSQ-105 Min	AD9433BSQ-105 Typ	AD9433BSQ-105 Max	AD9433BSQ-125 Min	AD9433BSQ-125 Typ	AD9433BSQ-125 Max	Unit
RESOLUTION				12			12		Bits
ACCURACY									
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Offset Error	Full	VI	–5	0	+5	–5	0	+5	mV
Gain Error[1]	25°C	I	–7	±1	+3	–7	±1	+3	% FS
Differential Nonlinearity (DNL)[2]	25°C	I	–0.75	±0.25	+0.75	–0.75	±0.3	+0.75	LSB
	Full	VI	–1		+1	–1		+1	LSB
Integral Nonlinearity (INL)[2]	25°C	I	–1.0	±0.5	+1.0	–1.0	±0.5	+1.0	LSB
	Full	VI	–1.3		+1.3	–1.3		+1.3	LSB
THERMAL DRIFT									
Offset Error	Full	V		–50			–50		ppm/°C
Gain Error[1]	Full	V		–125			–125		ppm/°C
Reference	Full	V		±80			±80		ppm/°C
REFERENCE									
Internal Reference Volatge (VREFOUT)	Full	I	2.4	2.5	2.6	2.4	2.5	2.6	V
Output Current (VREFOUT)	Full	V		100			100		µA
Input Current (VREFIN)	Full	IV			50			50	µA
ANALOG INPUTS									
Differential Input Voltage Range ($\overline{AIN}$, AIN)	Full	V		2.0			2.0		V
Common-Mode Voltage	Full	V		4.0			4.0		V
Input Resistance	Full	VI	2	3	4	2	3	4	kΩ
Input Capacitance	Full	V		4			4		pF
Analog Bandwidth, Full Power	Full	V		750			750		MHz
POWER SUPPLY									
V_{CC}	Full	IV	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{DD}	Full	IV	2.7		3.3	2.7		3.3	V
Power Dissipation[3]	Full	VI		1275	1425		1350	1500	mW
Power Supply Rejection Ratio (PSRR)	25°C	I		±3			±3		mV/V
IV_{CC}[2]	Full	VI		255	285		270	300	mA
IV_{DD}[2]	Full	VI		12.5	14		16	18	mA
ENCODE INPUTS									
Internal Common-Mode Bias	Full	V		3.75			3.75		V
Differential Input (ENC – $\overline{ENC}$)	Full	V		500			500		mV
Input Voltage Range	Full	IV	–0.5		V_{CC} + 0.05	–0.5		V_{CC} + 0.05	V
Input Common-Mode Range	Full	IV	2.0		4.25	2.0		4.25	V
Input Resistance	Full	VI		6			6		kΩ
Input Capacitance	25°C	V		3			3		pF
DIGITAL INPUTS									
Input High Voltage	Full	I	2.0			2.0			V
Input Low Voltage	Full	I			0.8			0.8	V
Input High Current (VIN = 5 V)	Full	V		50			50		µA
Input Low Current (VIN = 0 V)	Full	V		50			50		µA
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	V_{DD} – 0.05			V_{DD} – 0.05			V
Logic "0" Voltage	Full	VI			0.05			0.05	V
Output Coding				Two's Complement or Offset Binary					

NOTES

[1]Gain error and gain temperature coefficients are based on the ADC only (with a fixed 2.5 V external reference and a 2 V p-p differential analog input).

[2]SFDR disabled (SFDR = GND) for DNL and INL specifications.

[3]Power dissipation measured with rated encode and a dc analog input (Outputs Static, I_{VDD} = 0). I_{VCC} and I_{VDD} measured with 10.3 MHz analog input @ –0.5 dBFS.

Specifications subject to change without notice.

AC SPECIFICATIONS (V_{DD} = 3.3 V, V_{CC} = 5 V; differential encode input, unless otherwise noted.)

Parameter	Temp	Test Level	AD9433BSQ-105 Min	AD9433BSQ-105 Typ	AD9433BSQ-105 Max	AD9433BSQ-125 Min	AD9433BSQ-125 Typ	AD9433BSQ-125 Max	Unit
DYNAMIC PERFORMANCE*									
Signal-to-Noise Ratio (SNR)									
(Without Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	66.5	68.0		66.0	67.7		dB
f_{IN} = 49 MHz	25°C	I	65.5	67.5		64.0	66.0		dB
f_{IN} = 70 MHz	25°C	V		67.0			65.4		dB
f_{IN} = 150 MHz	25°C	V		65.4			62.0		dB
f_{IN} = 250 MHz	25°C	V		63.7			60.0		dB
Signal-to-Noise Ratio and Distortion (SINAD)									
(With Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	66.0	68.0		65.0	67.0		dB
f_{IN} = 49 MHz	25°C	I	64.0	67.5		63.5	65.5		dB
f_{IN} = 70 MHz	25°C	V		66.9			64.5		dB
f_{IN} = 150 MHz	25°C	V		64.0			61.5		dB
f_{IN} = 250 MHz	25°C	V		61.2			57.7		dB
Effective Number of Bits									
f_{IN} = 10.3 MHz	25°C	I		11.1			10.9		Bits
f_{IN} = 49 MHz	25°C	I		11.0			10.7		Bits
f_{IN} = 70 MHz	25°C	V		10.9			10.6		Bits
f_{IN} = 150 MHz	25°C	V		10.4			10.0		Bits
f_{IN} = 250 MHz	25°C	V		9.9			9.4		Bits
2nd and 3rd Harmonic Distortion									
f_{IN} = 10.3 MHz	25°C	I	–78	–85		–76	–85		dBc
f_{IN} = 49 MHz	25°C	I	–73	–80		–72	–76		dBc
f_{IN} = 70 MHz	25°C	V		–83			–78		dBc
f_{IN} = 150 MHz	25°C	V		–72			–67		dBc
f_{IN} = 250 MHz	25°C	V		–67			–65		dBc
Worst Other Harmonic or Spur									
(Excluding Second and Third)									
f_{IN} = 10.3 MHz	25°C	I	–88	–92		–84	–90		dBc
f_{IN} = 49 MHz	25°C	I	–82	–89		–82	–87		dBc
f_{IN} = 70 MHz	25°C	V		–87			–85		dBc
f_{IN} = 150 MHz	25°C	V		–87			–84		dBc
f_{IN} = 250 MHz	25°C	V		–85			–76		dBc
Two-Tone Intermod Distortion (IMD3)									
f_{IN1} = 49.3 MHz, f_{IN2} = 50.3 MHz	25°C	V		–92			–90		dBc
f_{IN1} = 150 MHz, f_{IN2} = 151 MHz	25°C	V		–80			–76		dBc

*SNR/Harmonics based on an analog input voltage of –0.5 dBFS referenced to a 2 V full-scale input range. Harmonics are specified with the SFDR active (SFDR = +5 V). SNR/SINAD specified with SFDR disabled (SFDR = Ground).

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (V_{DD} = 3.3 V, V_{CC} = 5 V; differential encode input, unless otherwise noted.)

Parameter	Temp	Test Level	AD9433BSQ-105 Min	AD9433BSQ-105 Typ	AD9433BSQ-105 Max	AD9433BSQ-125 Min	AD9433BSQ-125 Typ	AD9433BSQ-125 Max	Unit
Encode Rate	Full	IV	10		105	10		125	MSPS
Encode Pulsewidth High (t_{EH})	Full	IV	2.9			2.4			ns
Encode Pulsewidth Low (t_{EL})	Full	IV	2.9			2.4			ns
Aperture Delay (t_A)	25°C	V		2.1			2.1		ns
Aperture Uncertainty (Jitter)[1]	25°C	V		0.25			0.25		ps rms
Output Valid Time (t_V)[2]	Full	VI	2.5	4.0		2.5	4.0		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		4.0	5.5		4.0	5.5	ns
Output Rise Time (t_R)	Full	V		2.1			2.1		ns
Output Fall Time (t_F)	Full	V		1.9			1.9		ns
Out of Range Recovery Time	25°C	V		2			2		ns
Transient Response Time	25°C	V		2			2		ns
Latency	Full	IV		10			10		Cycles

NOTES

[1]Aperture uncertainty includes contribution of the AD9433, crystal clock reference, and encode drive circuit.

[2]t_V and t_{PD} are measured from the transition points of the ENCODE input to the 50%/50% levels of the digital output swing. The digital output load during testing is not to exceed an ac load of 10 pF or a dc current of 50 μA. Rise and fall times measured from 10% to 90%.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Unit
ELECTRICAL			
V_{DD} Voltage	–0.5	+6.0	V
V_{CC} Voltage	–0.5	+6.0	V
Analog Input Voltage	–0.5	V_{CC} + 0.5	V
Digital Input Voltage	–0.5	V_{CC} + 0.5	V
Digital Output Current		20	mA
ENVIRONMENTAL			
Operating Temperature Range (Ambient)	–40	+85	°C
Maximum Junction Temperature		+150	°C
Storage Temperature Range (Ambient)	–65	+125	°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARCTERISTICS

Thermal Resitance

52-Lead PowerQuad® 4 LQFP_ED

θ_{JA} = 25°C/W, Soldered Heat Sink, No Airflow

θ_{JA} = 33°C/W, Unsoldered Heat Sink, No Airflow

θ_{JC} = 2°C/W, Bottom of Package (Heat Sink)

Simulated typical performance for 4-layer JEDEC board, horizontal orientation.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at 25°C and guaranteed by design and characterization at specified temperatures.

III Sample Tested Only

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at 25°C and guaranteed by design and characterization for industrial temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9433BSQ-105	–40°C to +85°C (Ambient)	52-Lead Plastic Thermally Enhanced Quad Flatpack	SQ-52
AD9433BSQ-125	–40°C to +85°C (Ambient)	52-Lead Plastic Thermally Enhanced Quad Flatpack	SQ-52
AD9433/PCB	25°C	Evaluation Board with AD9433BSQ-125 (Supports – 105 Evaluation)	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9433 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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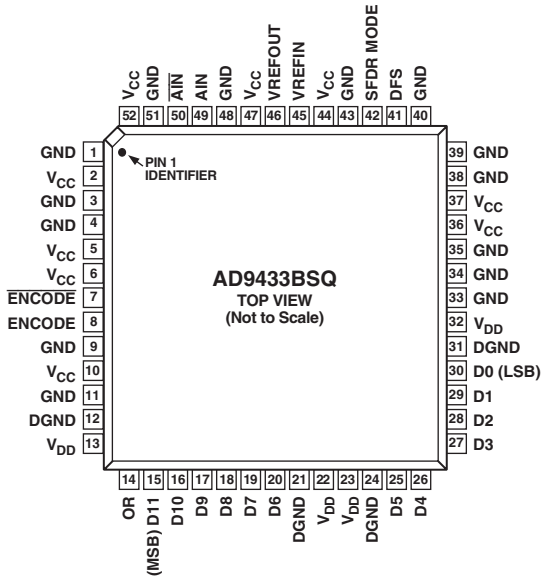
PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Function
1, 3, 4, 9, 11, 33, 34, 35, 38, 39, 40, 43, 48, 51	GND	Analog Ground
2, 5, 6, 10, 36, 37, 44, 47, 52	V_{CC}	Analog Supply (5 V)
7	$\overline{\text{ENCODE}}$	Encode Clock for ADC-Complementary
8	ENCODE	Encode Clock for ADC-True (ADC samples on rising edge of ENCODE)
14	OR	Out of Range Output
15–20, 25–30	D11–D0	Digital Output
13, 22, 23, 32	V_{DD}	Digital Output Power Supply (3 V)
12, 21, 24, 31	DGND	Digital Output Ground
41	DFS	Data Format Select. Low = Two's Complement, High = Binary; Floats Low
42	SFDR MODE	CMOS control pin that enables (SFDR MODE = 1), a proprietary circuit that may improve the spurious free dynamic range (SFDR) performance of the AD9433. It is useful in applications where the dynamic range of the system is limited by discrete spurious frequency content caused by nonlinearities in the ADC transfer function. SFDR MODE = 0 for normal operation; Floats Low.
45	VREFIN	Reference Input for ADC (2.5 V typical)
46	VREFOUT	Internal Reference Output (2.5 V typical); bypass with 0.1 µF to Ground
49	AIN	Analog Input-True
50	$\overline{\text{AIN}}$	Analog Input-Complement

PIN CONFIGURATION



DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a fullscale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak to peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits
The effective number of bits (ENOB) is calculated from the measured SNR based on the equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76\ dB + 20\ \log\left(\frac{Full\text{-}Scale\ Amplitude}{Input\ Amplitude}\right)}{6.02}$$

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in logic "1" state to achieve rated performance; pulsewidth low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a given clock rate, these specs define an acceptable Encode duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$Power_{Full\ Scale} = 10\ \log\left(\frac{\frac{V^2_{FullScale_{rms}}}{Z}}{0.001}\right)$$

Gain
Gain error is the difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion
The ratio of the rms signal amplitude fundamental frequency to the rms signal amplitude of a single harmonic component (second, third, etc.), reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best fit straight line determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The maximum encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a differential crossing of ENCODE and ENCODE and the time when all output data bits are within valid logic levels.

Noise (for Any Range within the ADC)

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}$$

Where *Z* is the input impedance, *FS* is the full scale of the device for the frequency in question, *SNR* is the value for the particular input level, and *SIGNAL* is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone (f_1, f_2) to the rms value of the worst third order intermodulation product; reported in dBc. Products are located at $2f_1 - f_2$ and $2f_2 - f_1$.

Two-Tone SFDR
The ratio of the rms value of either input tone (f_1, f_2) to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

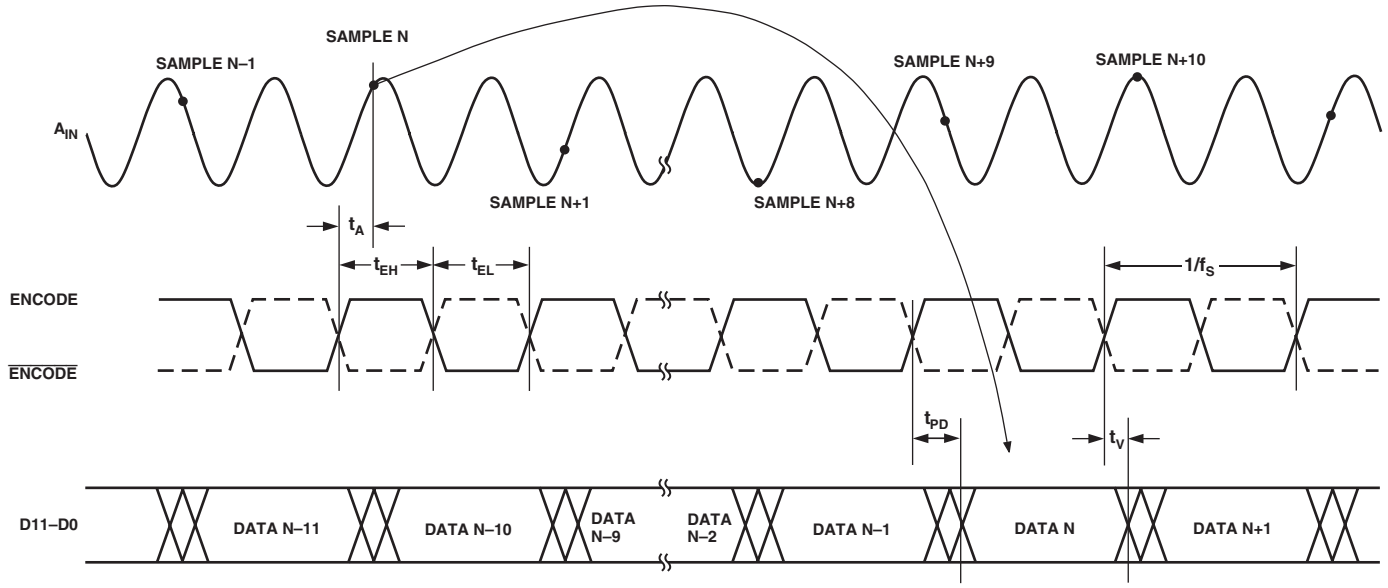


Figure 1. AD9433 Timing Diagram

EQUIVALENT CIRCUITS

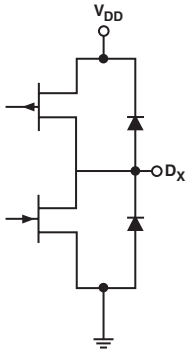


Figure 2. Digital Output

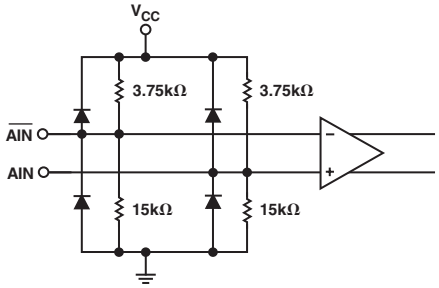


Figure 3. Analog Input

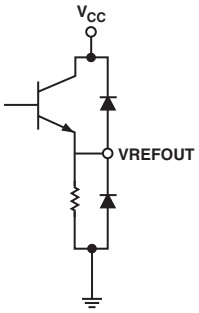


Figure 4. Reference Output

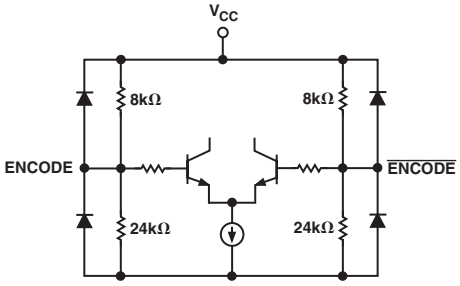


Figure 5. Encode Inputs

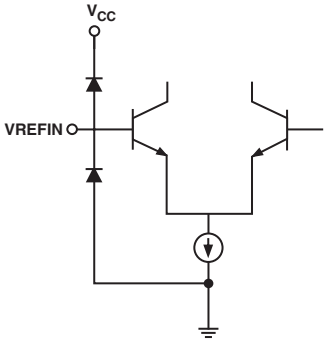
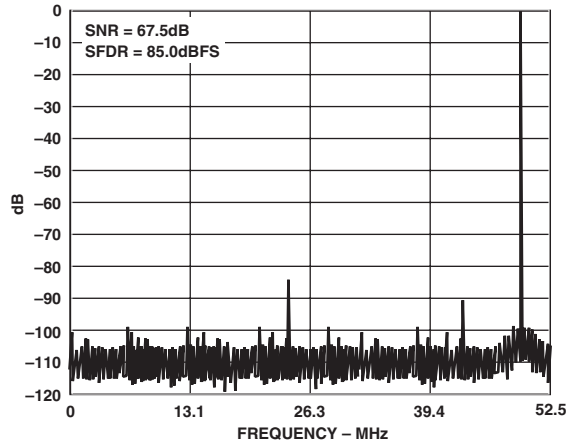
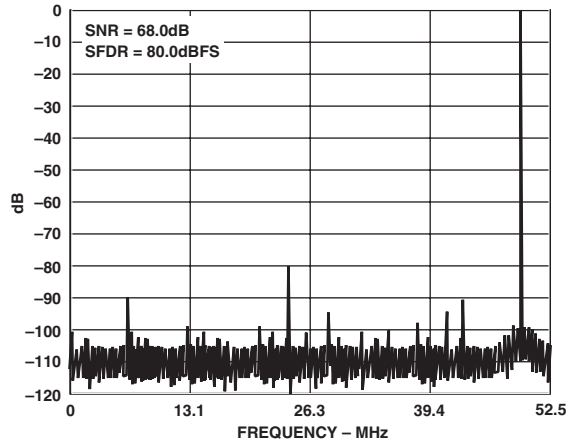


Figure 6. Reference Input

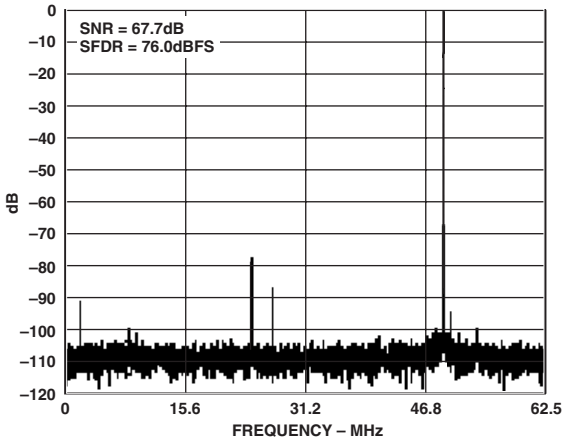
AD9433–Typical Performance Characteristics



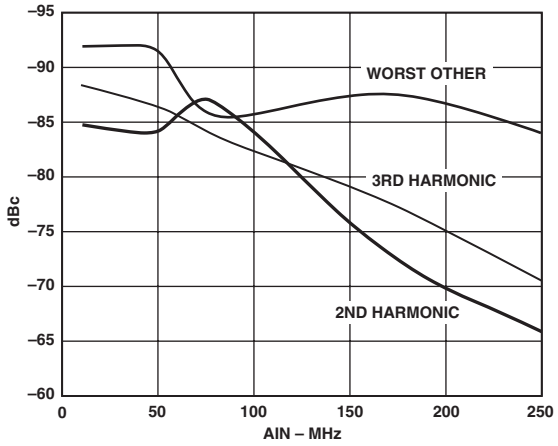
TPC 1. FFT: f_S = 105 MSPS, f_{IN} = 49.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



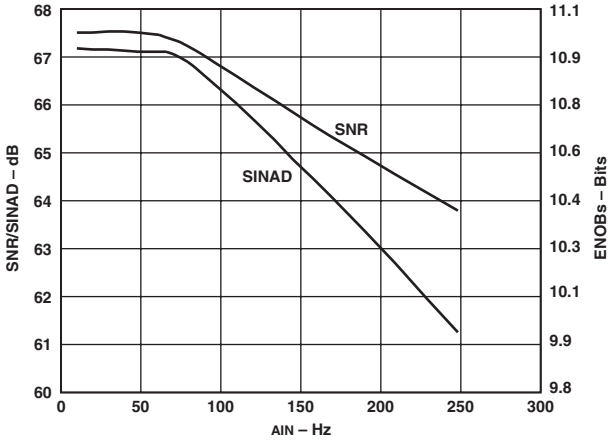
TPC 2. FFT: f_S = 105 MSPS, f_{IN} = 49.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Disabled



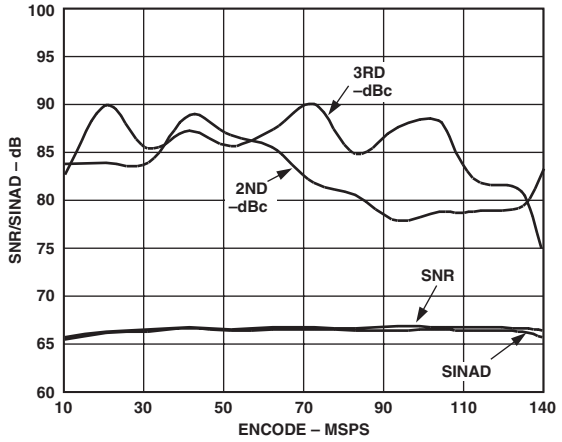
TPC 3. FFT: f_S = 125 MSPS, f_{IN} = 49.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



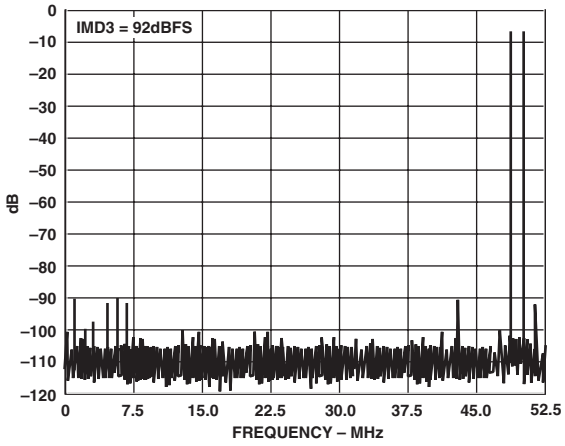
TPC 4. Harmonics (Second, Third, Worst Other) vs. AIN Frequency. AIN @ –0.5 dBFS, f_S = 105 MSPS, SFDR Enabled



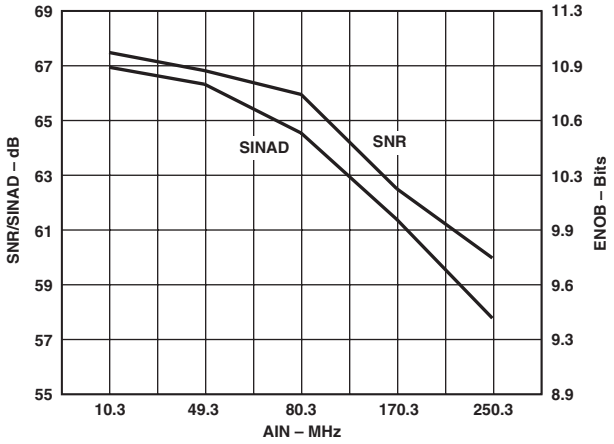
TPC 5. SNR vs. AIN Frequency. Differential AIN @ –0.5 dBFS, 105 MSPS, SFDR Disabled



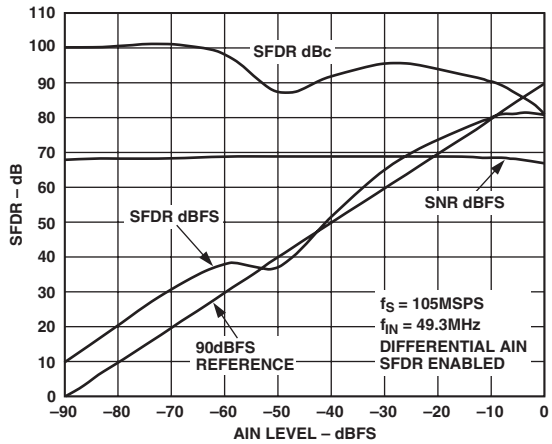
TPC 6. SNR/SINAD and Harmonic Distortion vs. Encode Frequency. Differential AIN @ –0.5 dBFS



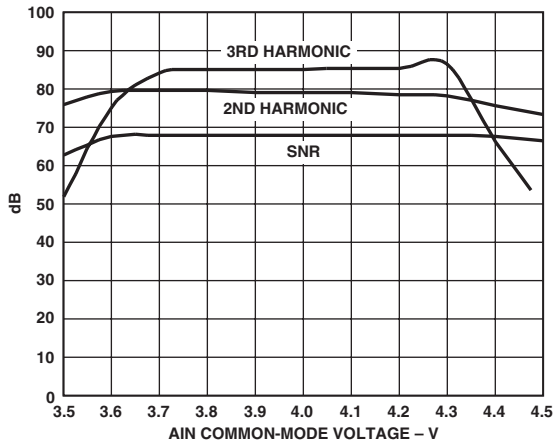
TPC 7. FFT: f_S = 105 MSPS, f_{IN} = 49.3 MHz and 50.3 MHz, Differential AIN @ –7 dBFS for Each Tone, SFDR Enabled



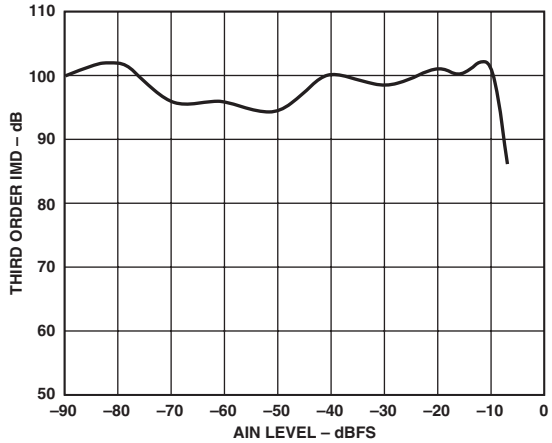
TPC 10. SNR and SINAD vs. AIN Frequency. Differential AIN @ –0.50 dBFS, f_S = 125 MSPS, SFDR Enabled



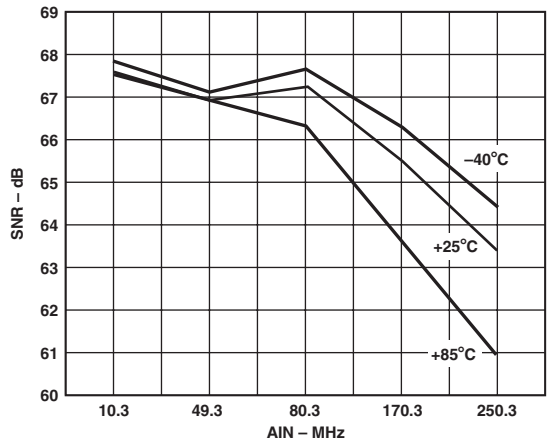
TPC 8. SNR and SFDR vs. AIN Level, f_S = 105 MSPS, f_{IN} = 49.3 MHz, Differential AIN, SFDR Enabled



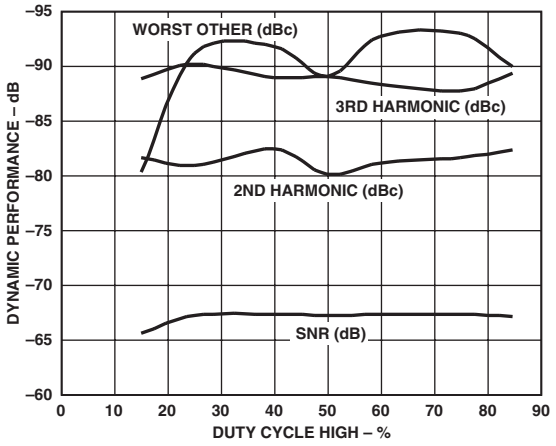
TPC 11. Dynamic Performance vs. AIN Common-Mode Voltage. Differential AIN @ –0.5 dBFS, f_{IN} = 49.3 MHz, f_S = 105 MSPS



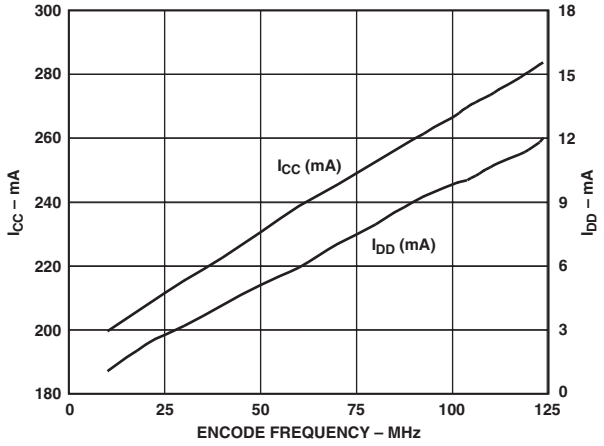
TPC 9. Third Order IMD vs. AIN Level, f_S = 105 MSPS, f_{IN} = 49.3 MHz and 50.3 MHz, Differential AIN, SFDR Enabled



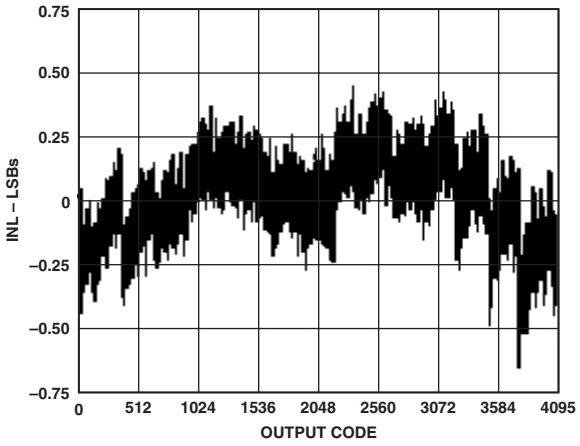
TPC 12. SNR vs. AIN Frequency/Temperature, f_S = 105 MSPS, Differential AIN, SFDR Disabled



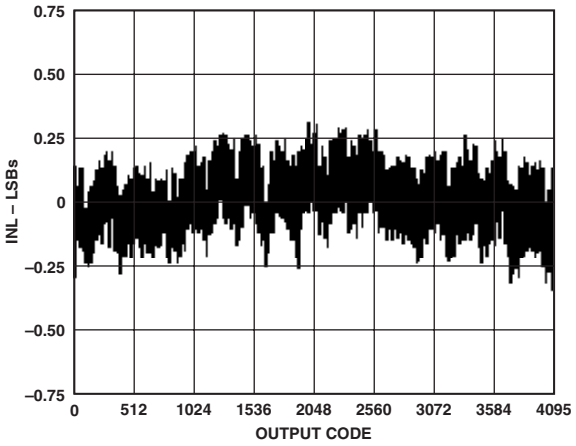
TPC 13. Dynamic Performance vs. Encode Duty Cycle f_S = 105 MSPS, f_{IN} = 49.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



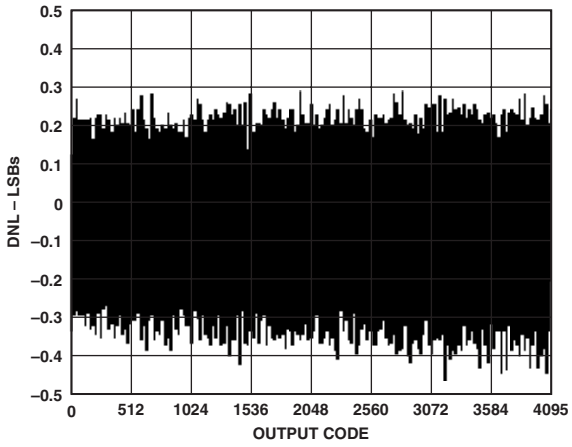
TPC 16. I_{DD} and I_{CC} vs. Encode Rate. f_{IN} = 10.3 MHz, Differential AIN @ –0.5 dBFS



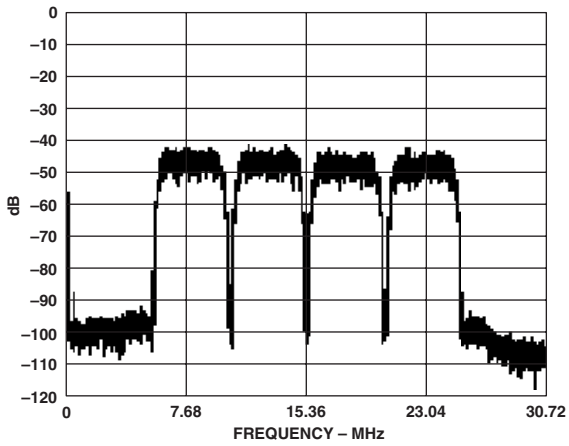
TPC 14. Integral Nonlinearity vs. Output Code with SFDR Disabled



TPC 17. Integral Nonlinearity vs. Output Code with SFDR Enabled

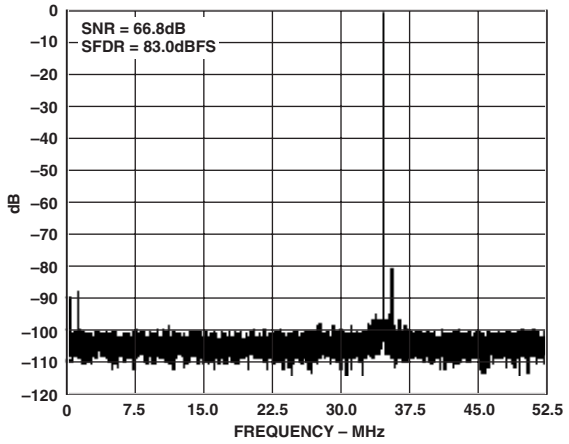


TPC 15. Differential Nonlinearity vs. Output Code

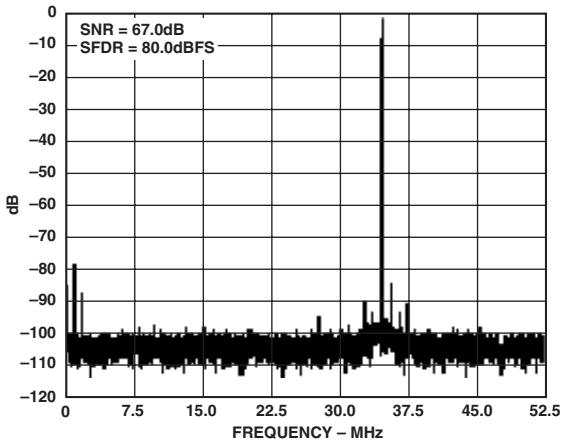


TPC 18. FFT: f_S = 61.44 MSPS, f_{IN} = 46.08 MHz, 4 WCDMA Carriers, Differential AIN, SFDR Enabled

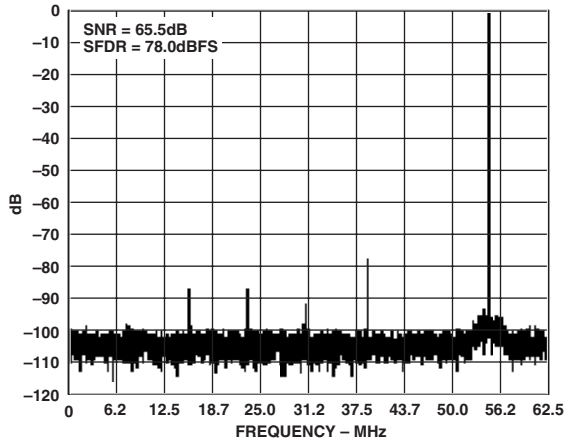
TYPICAL IF SAMPLING PERFORMANCE



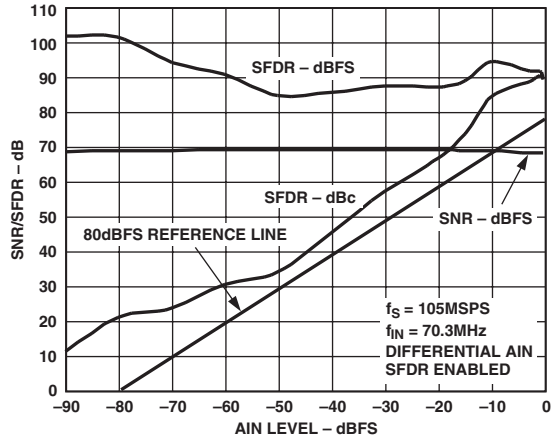
TPC 19. FFT: f_S = 105 MSPS, f_{IN} = 70.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



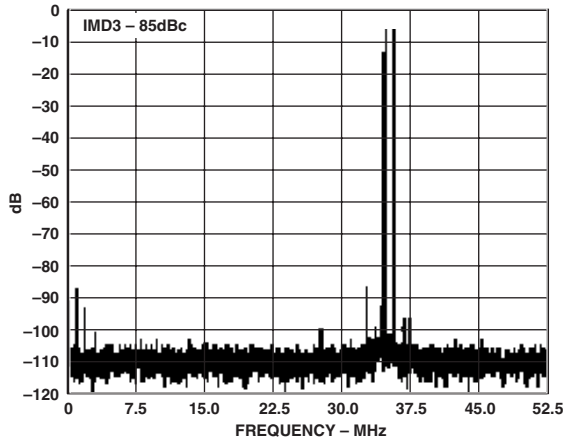
TPC 22. FFT: f_S = 105 MSPS, f_{IN} = 70.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Disabled



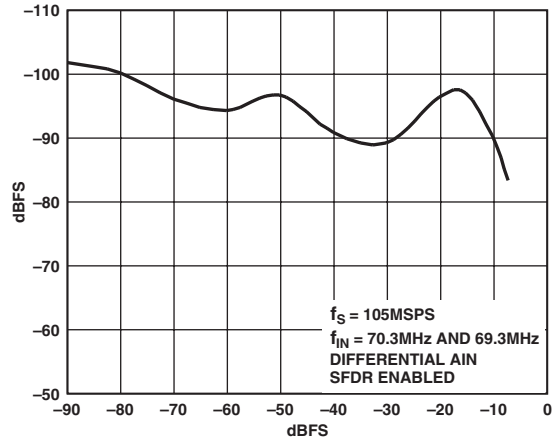
TPC 20. FFT: f_S = 125 MSPS, f_{IN} = 70.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



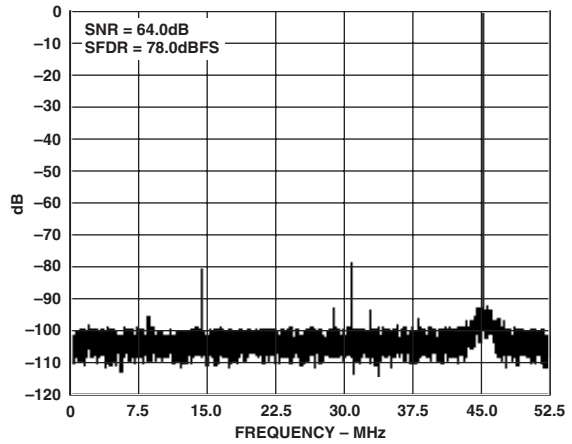
TPC 23. SNR/SFDR vs. AIN Level



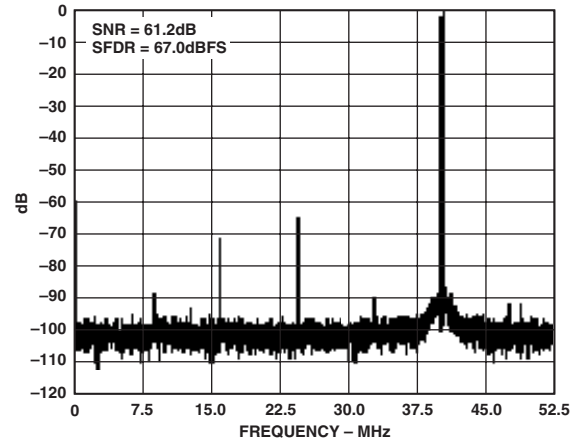
TPC 21. FFT: f_S = 105 MSPS, f_{IN} = 69.3 and 70.3 MHz, Differential AIN @ –7 dBFS for Each Tone, SFDR Enabled



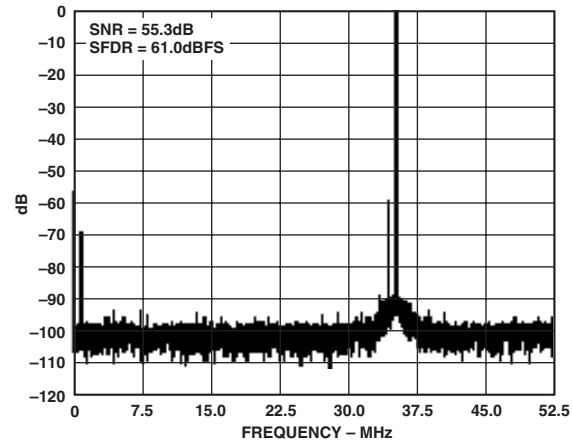
TPC 24. Third Order IMD vs. AIN Level, f_S = 105 MSPS, f_{IN} = 70.3 MHz and 69.3 MHz, Differential AIN, SFDR Enabled



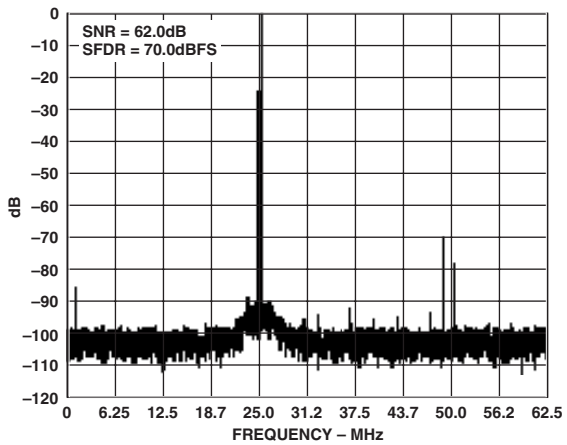
TPC 25. FFT: f_S = 105 MSPS, f_{IN} = 150.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



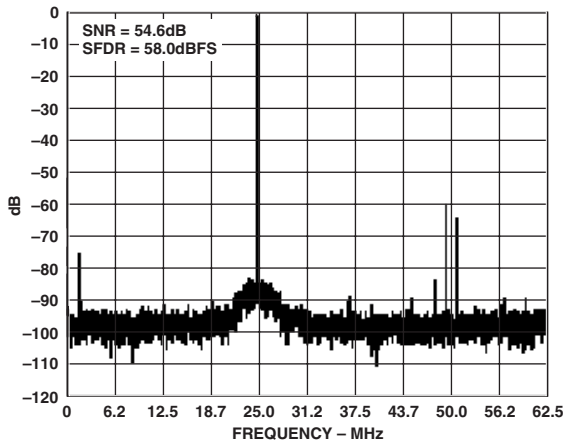
TPC 26. FFT: f_S = 105 MSPS, f_{IN} = 250.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



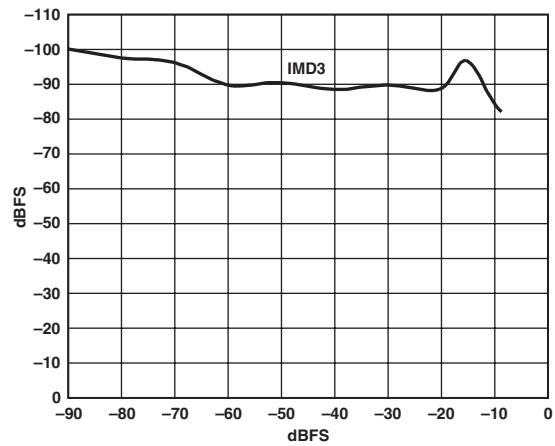
TPC 27. FFT: f_S = 105 MSPS, f_{IN} = 350.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



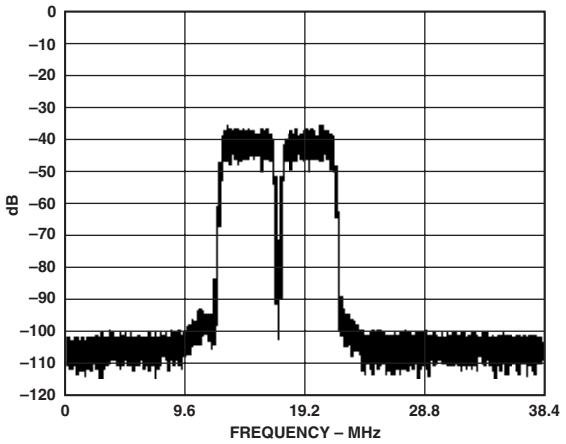
TPC 28. FFT: f_S = 125 MSPS, f_{IN} = 150.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



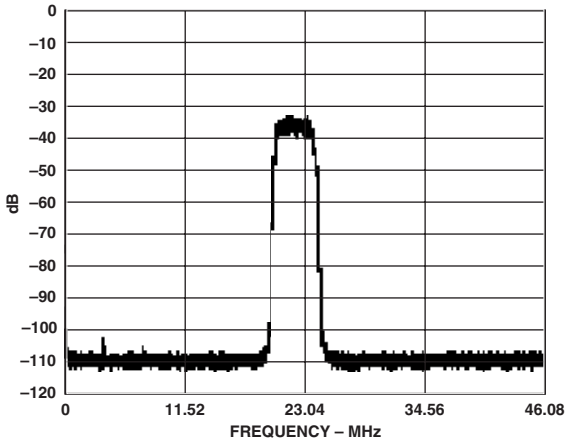
TPC 29. FFT: f_S = 125 MSPS, f_{IN} = 350.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Enabled



TPC 30. Third Order IMD vs. AIN Level, f_S = 105 MSPS, f_{IN} = 150.3 and 151.3 MHz, Differential AIN, SFDR Enabled



TPC 31. FFT: f_S = 76.8 MSPS, f_{IN} = 59.6 MHz, 2 WCDMA Carriers, Differential AIN, SFDR Enabled



TPC 32. FFT: f_S = 92.16 MSPS, f_{IN} = 70.3 MHz, WCDMA @ 70.0 MHz, SFDR Enabled

APPLICATION NOTES

Theory of Operation

The AD9433 is a multibit pipeline converter that uses a switched capacitor architecture. Optimized for high speed, this converter provides flat dynamic performance up to and beyond the Nyquist limit. DNL transitional errors are calibrated at final test to a typical accuracy of 0.25 LSB or less.

USING THE AD9433

ENCODE Input

Any high-speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track/hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9433, and the user is advised to give commensurate thought to the clock source.

The AD9433 has an internal clock duty cycle stabilization circuit that locks to the rising edge of ENCODE (falling edge of $\overline{\text{ENCODE}}$ if driven differentially), and optimizes timing internally. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern, and is not reduced by the internal stabilization circuit. This circuit is always on, and cannot be disabled by the user.

The ENCODE and $\overline{\text{ENCODE}}$ inputs are internally biased to 3.75 V (nominal), and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. Good performance is obtained using an MC10EL16 in the circuit to directly drive the encode inputs, as illustrated in Figure 7.

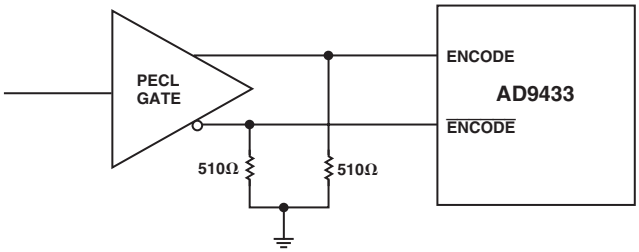


Figure 7. Using PECL to Drive the $\overline{\text{ENCODE}}$ Inputs

Often, the cleanest clock source is a crystal oscillator producing a pure, single-ended sine wave. In this configuration, or with any roughly symmetrical, single-ended clock source, the signal can be ac-coupled to the ENCODE input. To minimize jitter, the signal amplitude should be maximized within the input range described in Table I below. The 12 kΩ resistors to ground at each of the inputs, in parallel with the internal bias resistors, set the common-mode voltage to approximately 2.5 V, allowing the maximum swing at the input. The $\overline{\text{ENCODE}}$ input should be bypassed with a capacitor to ground to reduce noise. This ensures that the internal bias voltage is centered on the encode signal. For best dynamic performance, impedances at ENCODE and $\overline{\text{ENCODE}}$ should match.

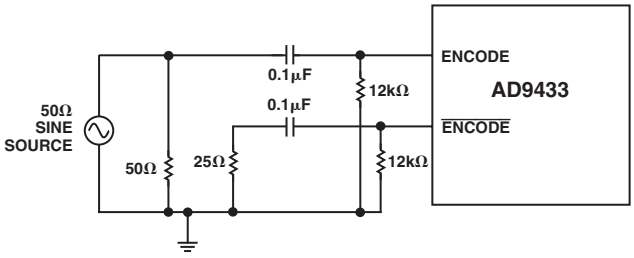


Figure 8. Single-Ended Sine Source Encode Circuit

Shown in Figure 9 is another preferred method for clocking the AD9433. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9433 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to the other portions of the AD9433, and limits the noise presented to the ENCODE inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limiting resistor (typically 100 Ω) is placed in the series with the primary.

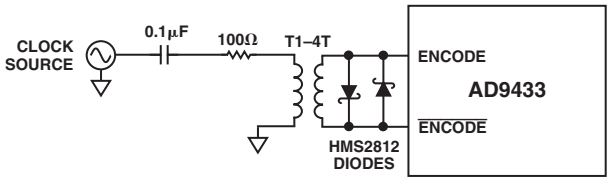


Figure 9. Transformer-Coupled Encode Circuit

ENCODE Voltage Level Definition

The voltage level definitions for driving ENCODE and $\overline{\text{ENCODE}}$ in single-ended and differential mode are shown in Figure 10.

Table I. ENCODE Inputs

Description	Minimum	Nominal	Maximum
Differential Signal Amplitude (V_{ID})	200 mV	750 mV	5.5 V
Input Voltage Range (V_{IHD}, V_{ILD}, V_{IHS}, V_{ILS})	–0.5 V		V_{CC} + 0.5 V
Internal Common-Mode Bias (V_{ICM})		3.750 V	
External Common-Mode Bias (V_{ECM})	2.0 V		4.25 V

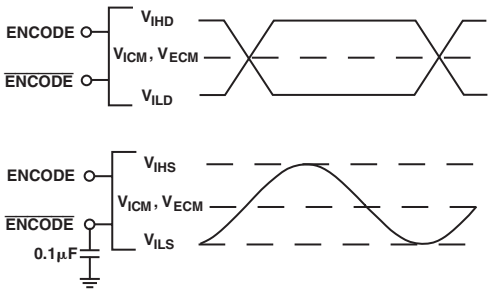


Figure 10. Differential and Single-Ended Input Levels

Analog Input

The analog input to the AD9433 is a differential buffer. The input buffer is self-biased by an on-chip resistor divider that nominally sets the dc common-mode voltage to 4 V (see Equivalent Circuits section). Rated performance is achieved by driving the input differentially. Minimum input offset voltage is obtained when driving from a source with a low differential source impedance, such as a transformer, in ac applications (See Figure 11). Capacitive coupling at the inputs will increase the input offset voltage by as much as 50 mV.

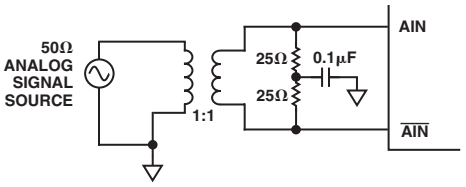


Figure 11. Transformer-Coupled Analog Input Circuit

In the highest frequency applications, two transformers connected in series may be necessary to minimize even-order harmonic distortion. The first transformer will isolate and convert the signal to a differential signal, but the grounded input on the primary side will degrade amplitude balance on the secondary winding. Capacitive coupling between the windings causes this imbalance. Since one input to the first transformer is grounded, there is little or no capacitive coupling, resulting in an amplitude mismatch at the first transformers output. A second transformer will improve the amplitude balance, and thus improve the harmonic distortion. A wideband transformer, such as the ADT1-1WT from Mini Circuits, is recommended for these applications, as the bandwidth through the two transformers will be reduced by the $\sqrt{2}$.

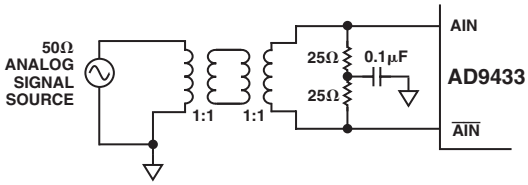


Figure 12. Driving the Analog Input with Two Transformers for Improved Even-Order Harmonics

Driving the ADC single-endedly will degrade performance, particularly even-order harmonics. For best dynamic performance, impedances at AIN and $\overline{\text{AIN}}$ should match.

Special care was taken in the design of the analog input section of the AD9433 to prevent damage and corruption of data when the input is overdriven.

SFDR Optimization

The SFDR MODE pin enables (SFDR MODE = 1) a proprietary circuit that may improve the spurious free dynamic range (SFDR) performance of the AD9433. It is useful in applications where the dynamic range of the system is limited by discrete spurious frequency content caused by nonlinearities in the ADC transfer function.

Enabling this circuit will give the circuit a dynamic transfer function, meaning that the voltage threshold between two adjacent output codes may change from clock cycle to clock cycle. While improving spurious frequency content, this dynamic aspect of the transfer function may be inappropriate for some time domain applications of the converter. Connecting the SFDR MODE pin to ground will disable this function. The typical performance curves section of the data sheet illustrates the improvement in the linearity of the converter and its effect on spurious free dynamic range (TPC 1, 2, 15, 18).

Digital Outputs

The digital outputs are 3 V (2.7 V to 3.3 V) TTL/CMOS-compatible for lower power consumption. The output data format is selectable through the data format select (DFS) CMOS input. DFS = 1 selects offset binary; DFS = 0 selects two's complement coding.

Table II. Offset Binary Output Coding (DFS = 1, V_{REF} = 2.5 V)

Code	AIN – $\overline{AIN}$ (V) Range = 2 V p-p	Digital Output
4095	+1.000	1111 1111 1111
•	•	•
•	•	•
2048	0	1000 0000 0000
2047	–0.00049	0111 1111 1111
•	•	•
•	•	•
0	–1.000	0000 0000 0000

Table III. Two's Complement Output Coding (DFS = 0, V_{REF} = 2.5 V)

Code	AIN – $\overline{AIN}$ (V) Range = 2 V p-p	Digital Output
+2047	+1.000	0111 1111 1111
•	•	•
•	•	•
0	0	0000 0000 0000
–1	–0.00049	1111 1111 1111
•	•	•
•	•	•
–2048	–1.000	1000 0000 0000

Voltage Reference

A stable and accurate 2.5 V voltage reference is built into the AD9433 (VREFOUT). In normal operation the internal reference is used by strapping Pin 45 to Pin 46 and placing a 0.1 μF decoupling capacitor at VREFIN. The input range can be adjusted by varying the reference voltage applied to the AD9433. No appreciable degradation in performance occurs when the reference is adjusted to 50. The full-scale range of the ADC tracks reference voltage changes linearly.

Timing

The AD9433 provides latched data outputs, with 10 pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (see Timing Diagram). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9433; these transients can detract from the converter's dynamic performance. The minimum guaranteed conversion rate of the AD9433 is 10 MSPS. At internal clock rates below 10 MSPS, dynamic performance may degrade.

Layout Information

The schematic and layout of the evaluation board (Figures 13–21) represents a typical implementation of the AD9433. A multilayer board is recommended to achieve best results. It is highly recommended that high quality, ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD9433 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs and their supply and ground pin connections are segregated to one side of the package, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD9433 (V_{CC}, AIN, and VREF), minimal capacitive loading should be placed on these outputs.

It is recommended that a fan-out of only one gate should be used for all AD9433 digital outputs.

The layout of the encode circuit is equally critical, and should be treated as an analog input. Any noise received on this circuitry will result in corruption in the digitization process and lower overall performance. The Encode clock must be isolated from the digital outputs and the analog inputs.

Replacing the AD9432 with the AD9433

The AD9433 is pin-compatible with the AD9432, although there are two control pins on the AD9433 that do not connect (DNC) and supply (V_{CC}) connections on the AD9432. They are summarized in the table below.

Table IV. AD9432/AD9433 Pin Differences

Pin	AD9432	AD9433
41	DNC	DFS
42	V_{CC}	SFDR MODE

Using the AD9433 in an AD9432 pin assignment will configure the AD9433 as follows:

- The SFDR improvement circuit will be enabled.
- The DFS pin will float LOW, selecting two's complement coding for the digital outputs, which is the same as the AD9432.

Table V summarizes differences between the AD9432 and AD9433 analog and encode input common-mode voltages. These inputs may be ac-coupled so that the devices can be used interchangeably.

Table V. Other AD9432/AD9433 Differences

Attribute	AD9432	AD9433
ENCODE/$\overline{ENCODE}$ $V_{COMMON\ MODE}$	1.6 V	3.75 V
AIN/$\overline{AIN}$ $V_{COMMON\ MODE}$	3.0 V	4.0 V

Table VI. Power Supply Connections for the AD9433 Evaluation Board

Connector	Pin	Designator	External Supply Required	Approximate Current Level
P42	P1, P3	GND	Ground	
	P2	–5 V (Optional U10 Supply)	–5 V	30 mA
	P4	V_{DL}	+3 V	144 mA
P43	P1, P3	GND	Ground	
	P2	V_O	+3 V	10 mA
	P4	V_{CC}	+5 V	325 mA Without U10 355 mA With U10

Evaluation Board

The AD9433 evaluation board offers designers an easy way to evaluate device performance. The user must supply an analog input signal, encode clock reference, and power supplies. The digital outputs of the AD9433 are latched on the evaluation board, and are available with a data ready signal at a 40-pin edge connector. Please refer to the evaluation board schematic, layout, and bill of materials that follow.

Power Connections

Power to the board is supplied via two detachable, four-pin power strips (P42 and P43). These eight pins should be driven as outlined in Table VI. Please note that the –5 V supply is optional, and only required if the user adds differential op amp U10 to the board.

Jumper Options

The table below describes the jumper options on the AD9433 Evaluation board.

Table VII. AD9433 Evaluation Board Jumper Options

Jumper Designation	Connection	Configuration
SFDR	5 V	SFDR Enhancement Circuit Enabled
	GND	SFDR Enhancement Circuit Disabled
DFS	5 V	Offset Binary Output Data Format
	GND	Two's Complement Output Data Storage
LATCH	E10 to E6	Output Register (U7–U8) Clock is Buffered
	E10 to E5	Output Register (U7–U8) Clock is Inverted
DATA READY	E7 to E8	Data Ready Signal is Buffered
	E7 to E9	Data Ready Signal is Inverted

Encode Signal and Distribution

The encode input signal should drive SMB connector P38, which has an on-board 50 Ω termination. This signal is ac-coupled, and may be either a low jitter pulse or a sine wave reference, with up to 4 V p-p amplitude. U2 (MC10EP16) converts this single-ended input signal to a differential PECL signal to drive the AD9433. U1 (DS90LV048A) also converts the signal at P38 to a CMOS level signal to drive the clock inputs of the two output data registers U7–U8, (74LVT574WM), the reconstruction DAC U3 (AD9772AAST), and the output data connector.

Analog Input

The analog input signal is ac-coupled to the evaluation board by SMB connector P39. Transformers T1 and T2 (ADT1-1WT) convert this signal to a differential signal to drive AIN and $\overline{\text{AIN}}$ of the AD9433. These RF transformers are specified as 1:1, but their turns ratio is actually 6:7. T1 is rotated 180° and mounted on the board such that its secondary and primary are reversed, making its ratio 7:6. The second transformer in series now form a combined 1:1 turns ration for the analog signal, and provide a 50 Ω termination for connector J1 via 25 Ω resistors R3 and R4. Resistor R3, normally omitted, can be used to terminate P39 if the transformers are removed for single ended drive. In this configuration, the user will need to short the input signal from Pin 3 of T1 to Pin 6 of T2, and remove resistor R4. Resistor R3 should remain in place to match the impedance of AIN and $\overline{\text{AIN}}$.

Using the AD8350

An optional driver circuit for the analog input, based on the AD8350 differential amplifier, is included in the layout of the AD9433 evaluation board. This portion of the evaluation circuit is not populated when the board is manufactured, but can be easily added by the user. Removing resistors R29 and R30 will disconnect the normal analog input signal path, and populating R17 and R31 will connect the AD8350 output network.

DAC Reconstruction Circuit

The data available at output connector U2 is also reconstructed by DAC U3, the AD772A. This 14-bit, high-speed digital-to-analog converter is included as a tool in setting up and debugging the evaluation board. It should not be used to measure the performance of the AD9433, as its performance will not accurately reflect the performance of the ADC. As configured on the AD9433 evaluation board, the AD9772A divides the input clock frequency by a factor of two, and ignores every other sample from the AD9433. The AD9772 internally interpolates the missing samples so that the DAC output will reflect the input of the AD9433 only when the analog input frequency is less than or equal to 1/4 the ADC encode rate. The AD9772 requires offset binary format so the DFS jumper should be connected to 5 V. The DAC's output, available at J1, will drive 50 Ω. The user may move the jumper wire between E43 and E42 to connect E43 to E44, thus activating the SLEEP function of the DAC.

Evaluation Board Bill of Materials

Item	Qty	Reference Designator	Device	Package	Value
1	1	AD9433/PCB	PCB		
2	1	U4	ADC	QFP52	AD9433BST-XXX
3	1	U3	DAC	LQFP48	AD9772AAST
4	1	U1	Quad LVDS/CMOS	SO16	DS90LV048A
5	1	U2	Diff. ECL Receiver	SO8NB	MC10EP16
6	2	U7–U8	D Flip-Flop		74LVT574WM
7	2	T1–T2	1:1 Transformer	CD542	ADT1-1WT
8	35	C1, C2, C4–C8, C10, C12–C18, C20–C24, C27–C28, C30–C38, C42–C43, C45, C48	Capacitor	0603A	0.1 µF
9	3	C9, C40–C41	Capacitor	BCAPTAJD	10 µF
10	1	C11	Capacitor	0603A	10 µF
11	2	R10, R23	BRES603	0603A	50 Ω
12	2	R29–R30	BRES603	0603A	33 Ω
13	4	R1–R2, R24–R25	BRES603	0603A	510 Ω
14	3	R3–R4, R7	BRES603	0603A	25 Ω
15	3	R6, R8, R14	BRES603	0603A	2 kΩ
16	2	R9, R13	BRES603	0603A	1.2 kΩ
17	2	R11, R16	BRES603	0603A	1 kΩ
18	1	R12	BRES603	0603A	220 Ω
19	2	RZ1–RZ2	Resistor Pack	SO16RES	742C163221 (220 Ω)
20	2	RZ4–RZ5	Resistor Pack	SO16RES	742C163220 (22 Ω)
21	3	J1, P38–P39	SMBPN	SMB	PC-Mount SMB
22	1	P44	40 Pin Header	C40MS	Samtec Tsw-120-07-G-D
23	2	P42–P43	Power Connector	PTMICRO4	Weiland Z5.531.3425.0 Posts 25.602.5453.0 Top
24	15	E5–E7, E8–E10, E19–E21, E25–E27, E31–E33	“E” Holes	Jumper Blocks	TSW-120-07-G-S SMT-100-BK-G
25	4	E28/E29, E36/E37, E39/E40, E42/E43	“E” Holes	Wire Straps	Short at Assembly
26*	1	T3	1:1 Transformer	CD543	ADT1-1WT
27*	1	U10	Op Amp	SO8	AD8350
28*	7	C3, C46–C47, C50–C53	Capacitor	0603A	0.1 µF
29*	1	C44	Capacitor	BCAPTAJD	10 µF
30*	2	R15, R27	BRES604	0603A	50 Ω
31*	2	R18–R19	BRES606	0603A	25 Ω
32*	2	R20, R33	BRES608	0603A	1.5 kΩ
33*	2	R21, R28	BRES605	0603A	100 Ω
34*	6	L1–L2, R17, R22, R31, C29, C49	Select (R, L, C)	0603A	Select
35*	1	P41	SMBPN	SMB	PC-Mount SMB
36*	6	E30, E34–E35, E38, E41, E44	“E” Holes	Option Holes	

*Items are included in the PCB design, but are omitted at assembly.

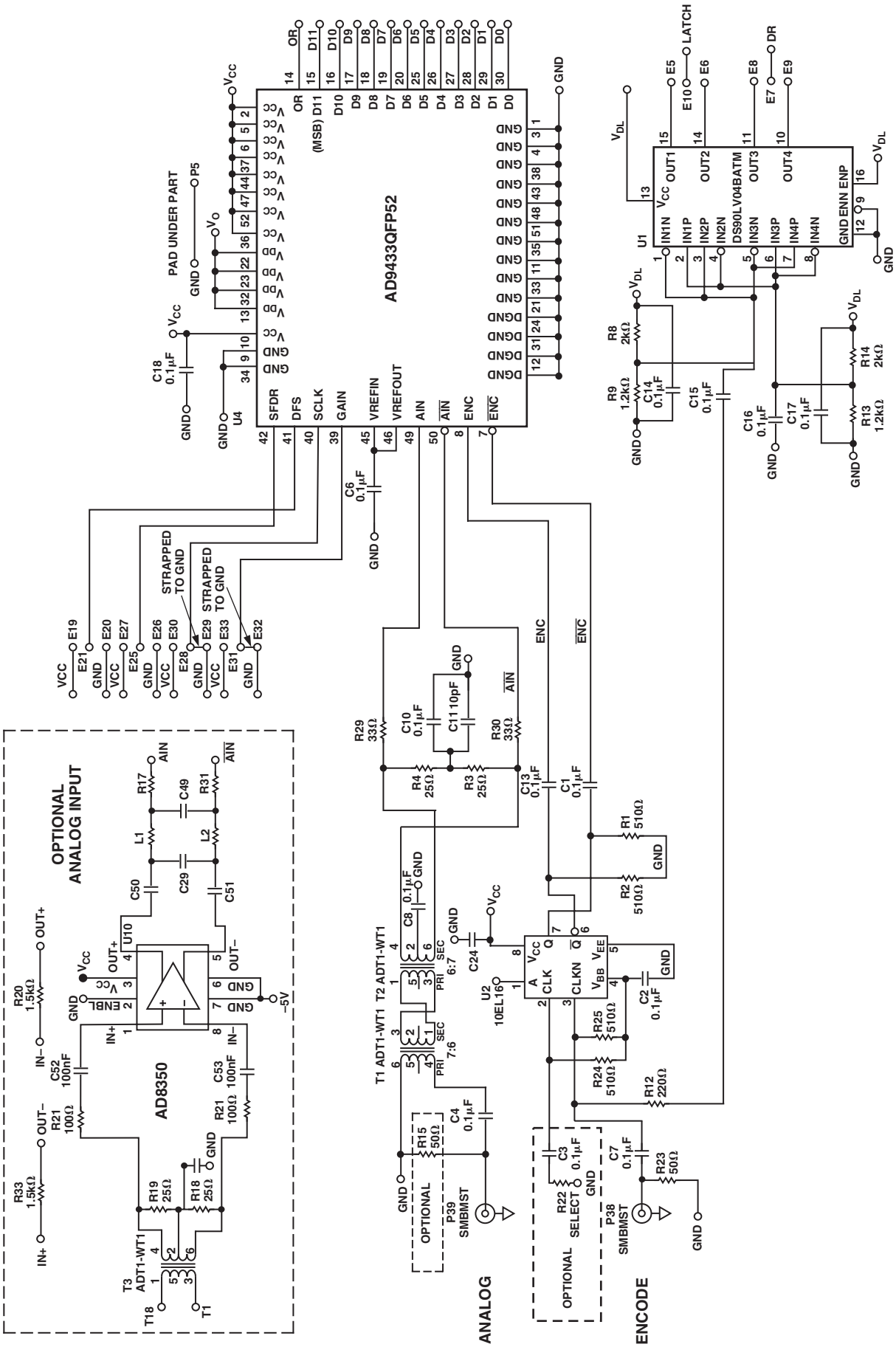


Figure 13. Evaluation Board Schematic

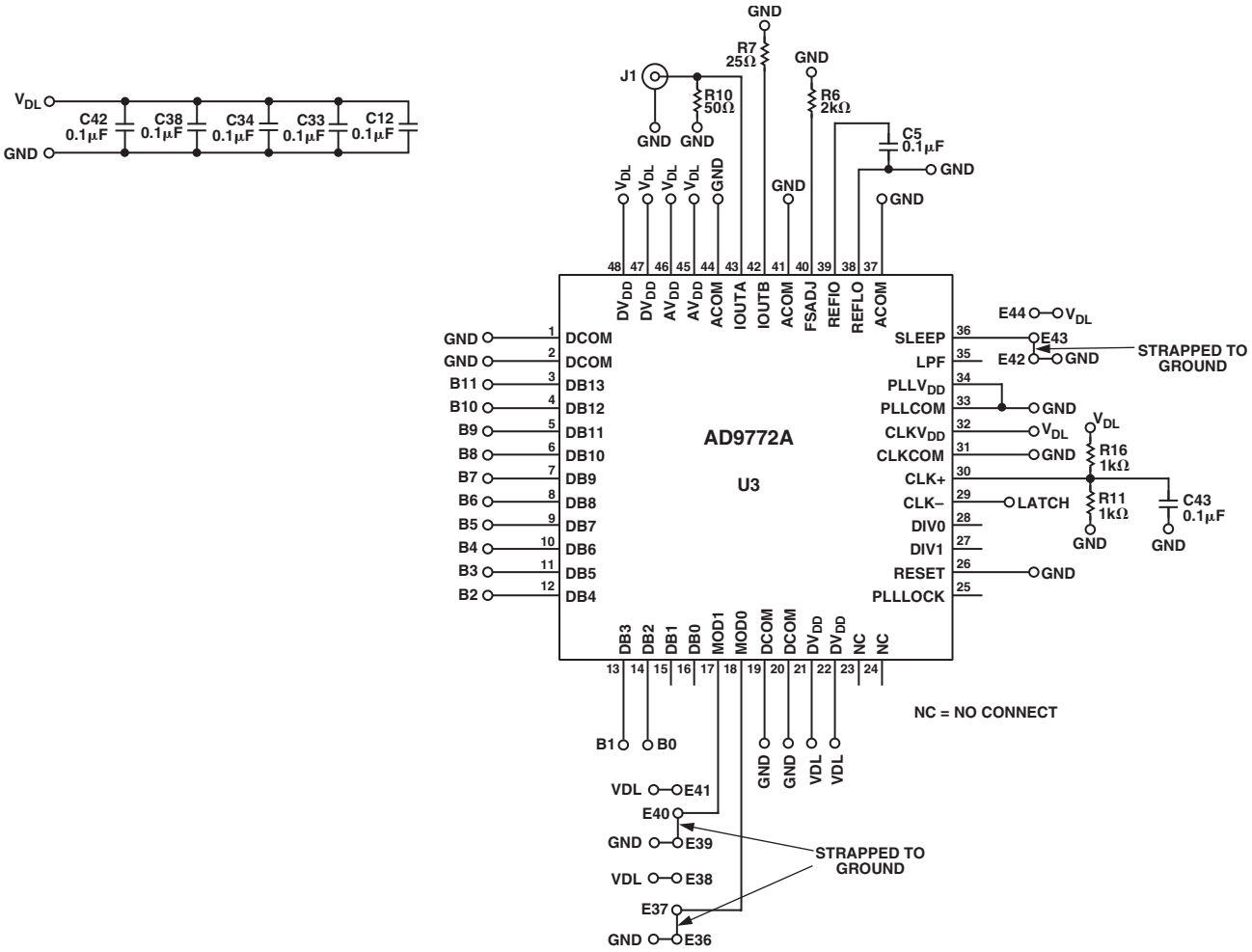


Figure 14. Evaluation Board Schematic

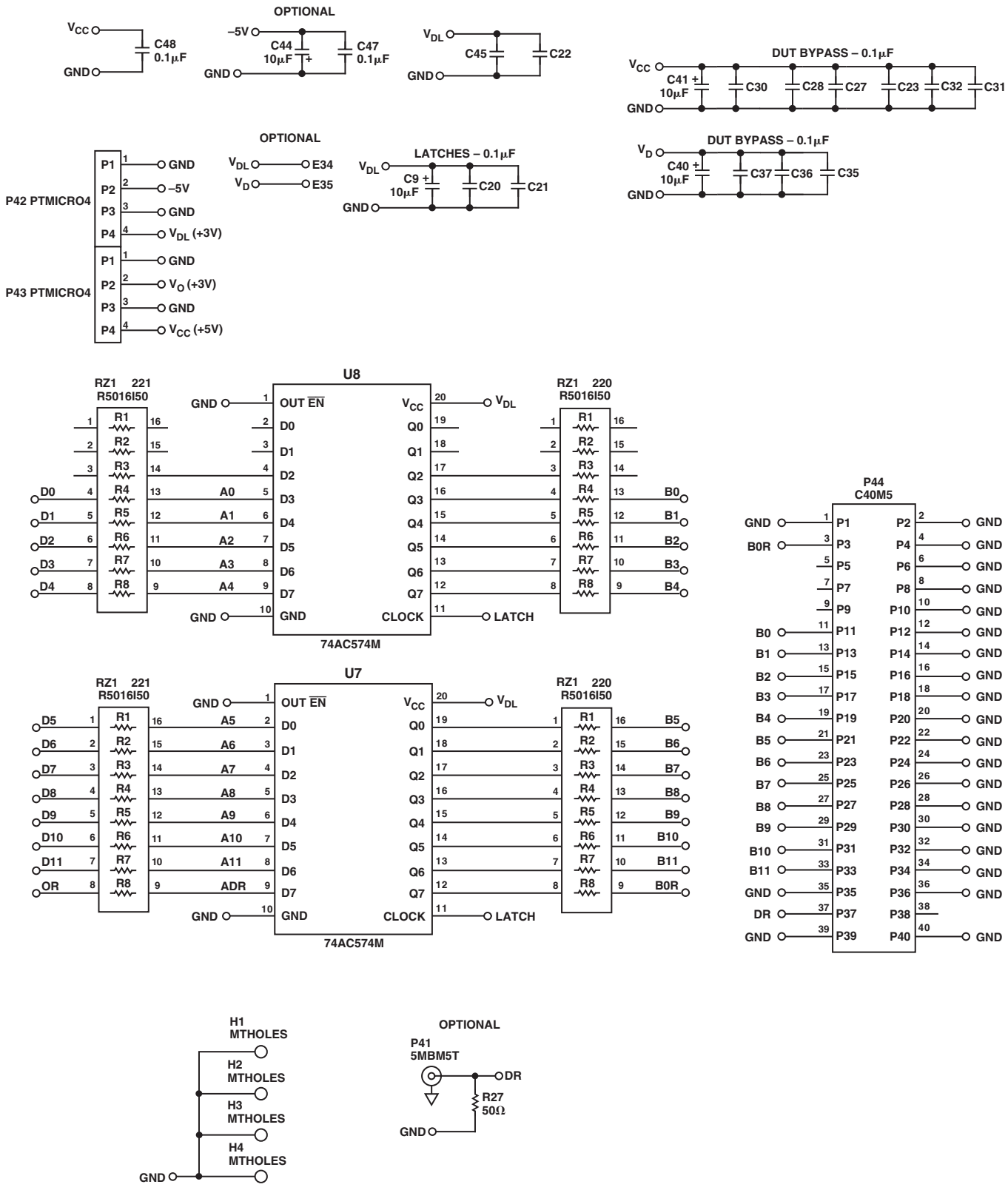


Figure 15. Evaluation Board Schematic

AD9433 EVALUATION BOARD LAYOUT

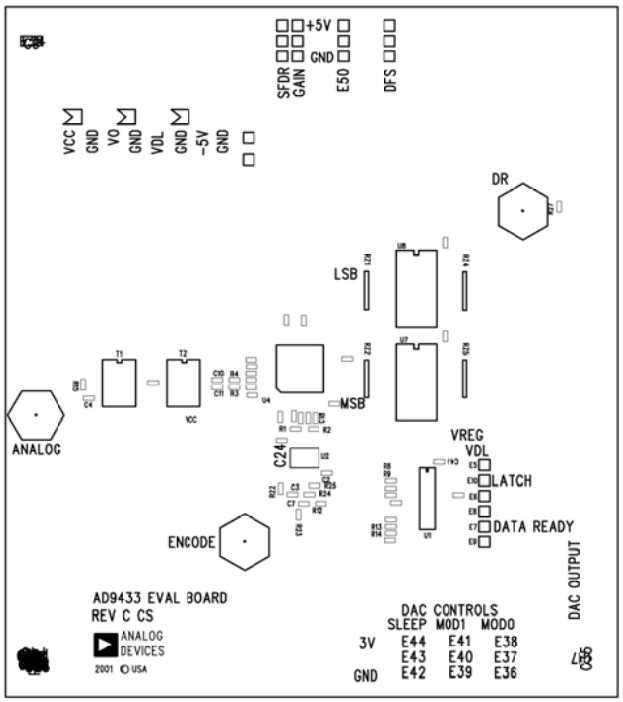


Figure 16. Top Silkscreen

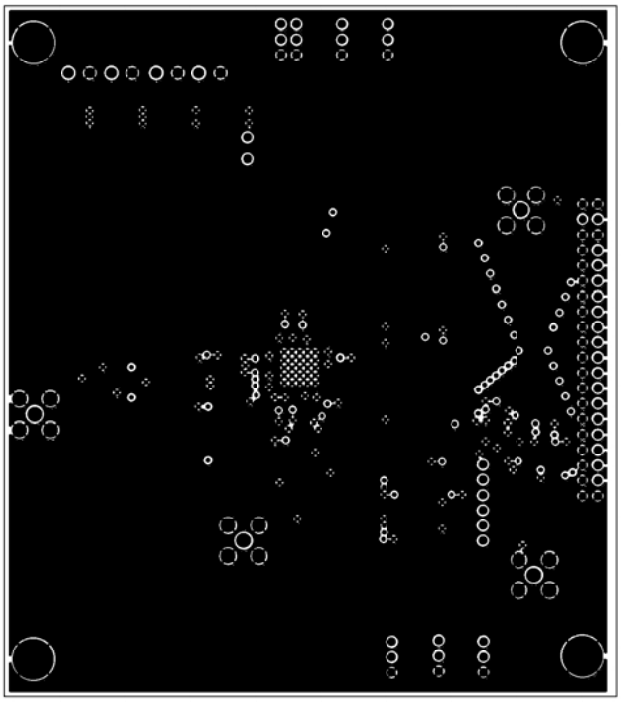


Figure 18. Ground Plane

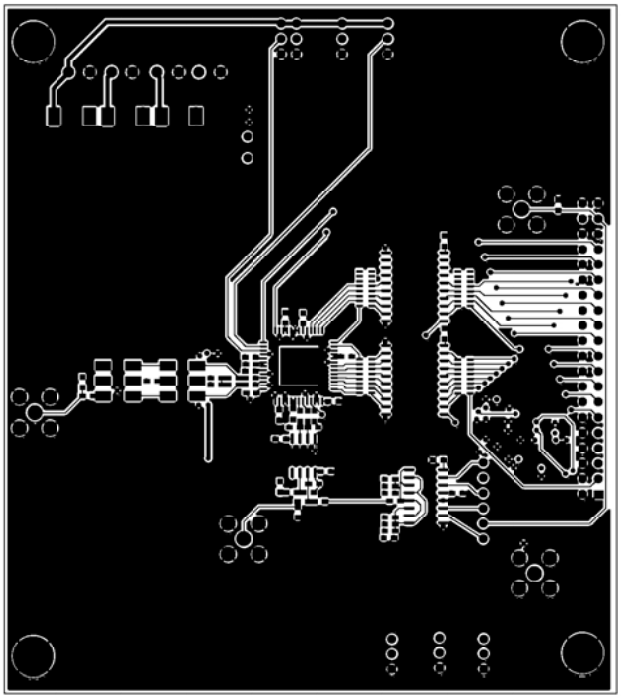


Figure 17. Top Level Routing

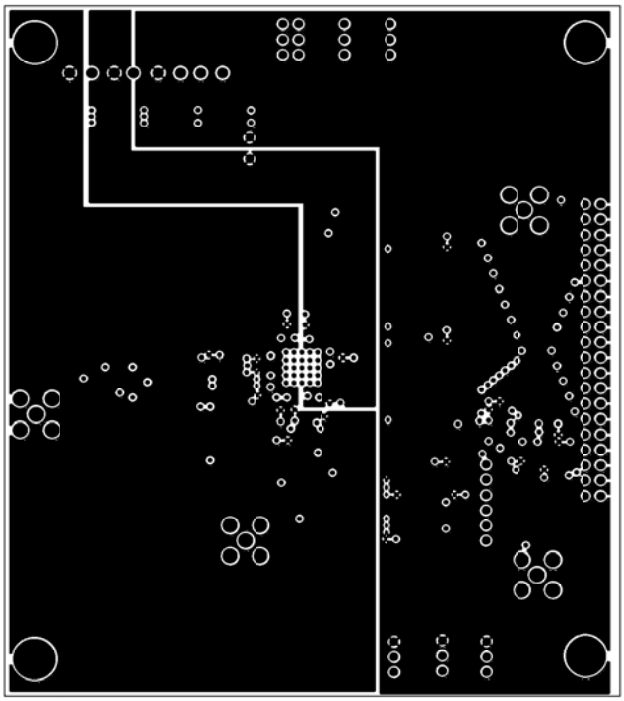


Figure 19. Power Plane

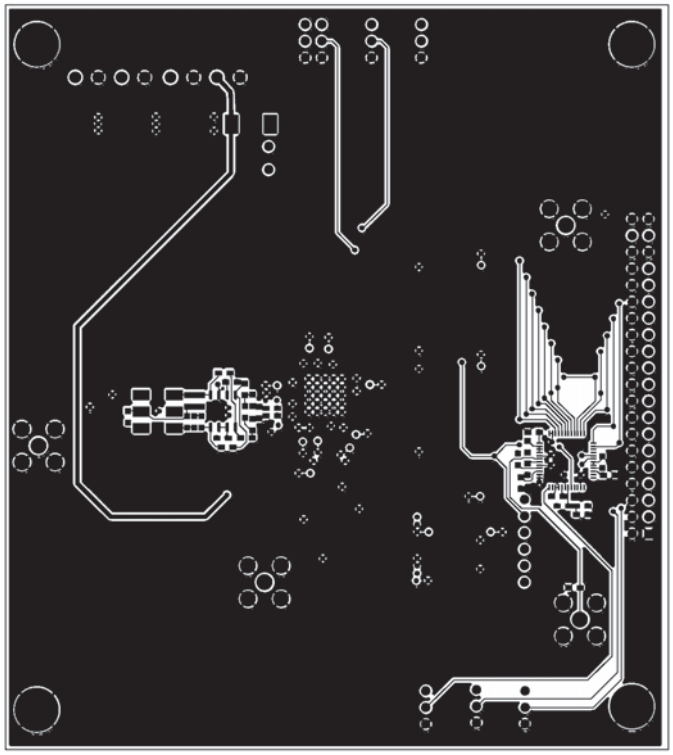


Figure 20. Bottom Layer Routing

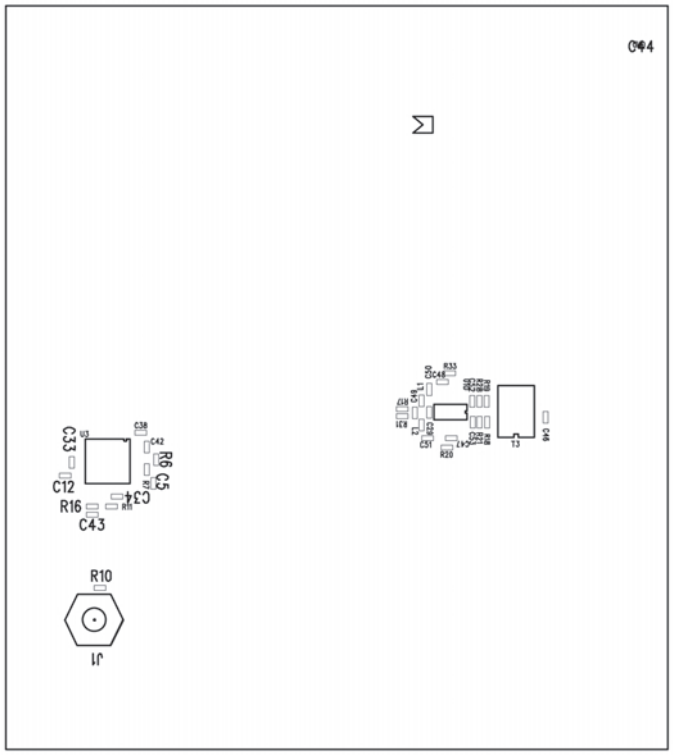
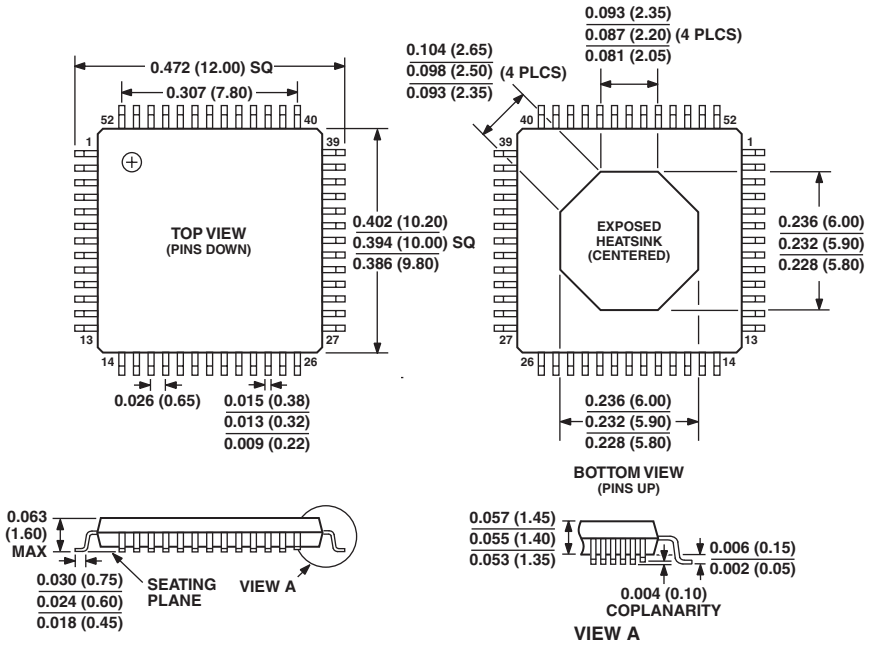


Figure 21. Bottom Silkscreen

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Thermally Enhanced
52-Lead Power Thin Plastic Quad Flatpack (LQFP_ED)
(SQ-52)



NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS. INCH DIMENSIONS ARE ROUNDED OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
2. ALTHOUGH NOT REQUIRED IN ALL APPLICATIONS, THE AD9433 HAS AN EXPOSED METALLIC PAD ON THE PACKAGE BOTTOM WHICH IS INTENDED TO ENHANCE THE HEAT REMOVAL PATH. TO MAXIMIZE THE REMOVAL OF HEAT, A LAND PATTERN WITH CLOSELY SPACED THERMAL VIAS TO THE GROUND PLANE(S) SHOULD BE INCORPORATED ON THE PCB WITHIN THE FOOTPRINT OF THE PACKAGE CORRESPONDING TO THE EXPOSED METAL PAD DIMENSIONS OF THE PACKAGE. THE SOLDERABLE LAND AREA SHOULD BE SOLDER MASK DEFINED AND BE AT LEAST THE SAME SIZE AND SHAPE AS THE EXPOSED PAD AREA ON THE PACKAGE. AT LEAST 0.25 MM CLEARANCE BETWEEN THE OUTER EDGES OF THE LAND PATTERN AND THE INNER EDGES OF THE PAD PATTERN SHOULD BE MAINTAINED TO AVOID ANY SHORTS.

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